

(A)

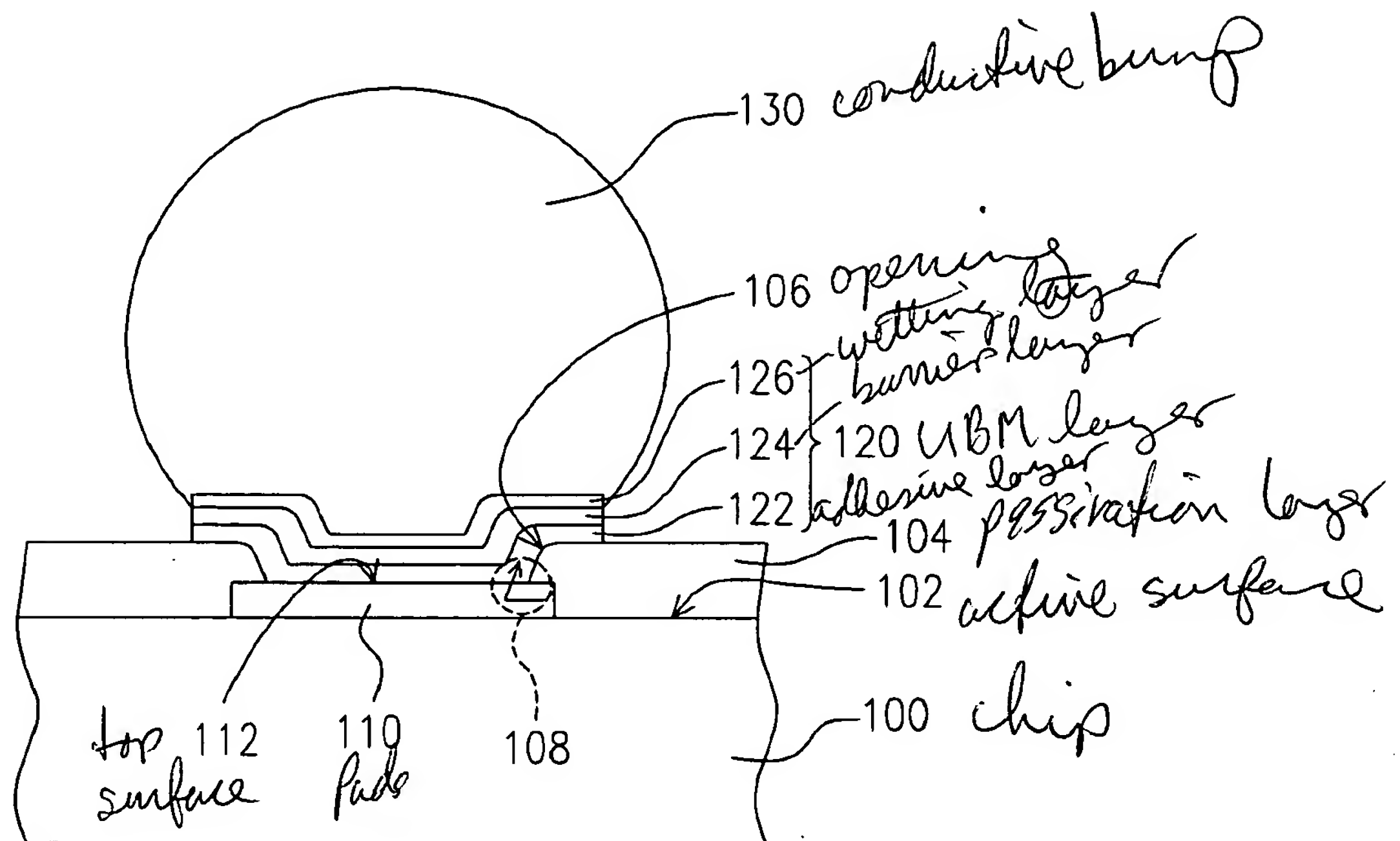


FIG. 1 (PRIOR ART)

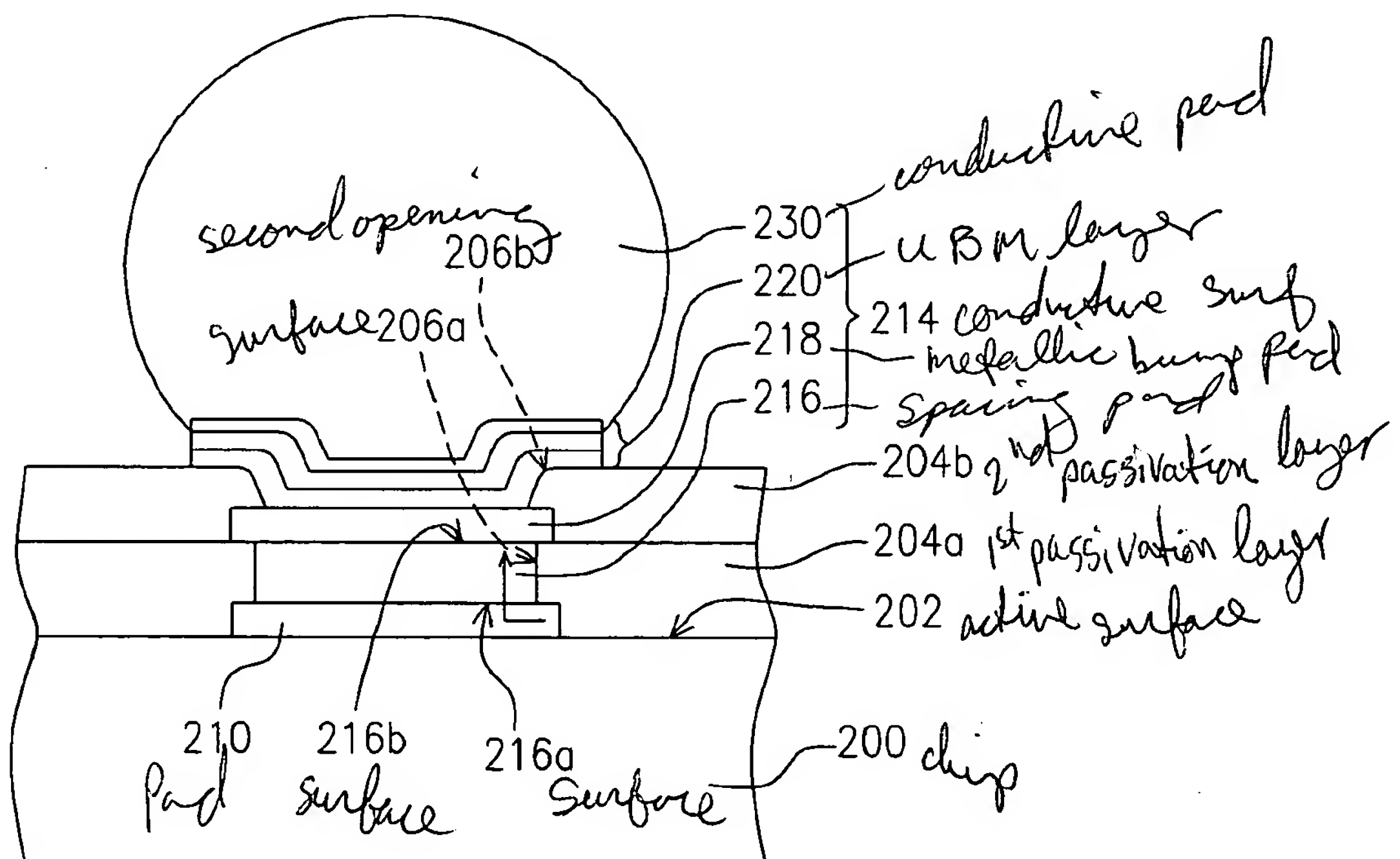


FIG. 2

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(12) **United States Patent**
Farnworth

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(54) **MASK REPATTERN PROCESS**

(75) Inventor: **Warren M. Farnworth, Nampa, ID (US)**

(73) Assignee: **Micron Technology, Inc., Boise, ID (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

(63) Continuation of application No. 10/017,419, filed on Dec. 12, 2001, now Pat. No. 6,555,460, which is a continuation of application No. 09/754,671, filed on Jan. 4, 2001, now Pat. No. 6,365,501, which is a continuation of application No. 09/464,988, filed on Dec. 16, 1999, now Pat. No. 6,211,052, which is a continuation of application No. 09/179,310, filed on Oct. 27, 1998, now Pat. No. 6,083,820, which is a continuation of application No. 08/767,162, filed on Dec. 16, 1996, now Pat. No. 5,851,911, which is a continuation-in-part of application No. 08/612,059, filed on Mar. 7, 1996, now Pat. No. 6,072,236, and a continuation-in-part of application No. 08/682,141, filed on Jul. 17, 1996, now Pat. No. 5,736,456.

(51) Int. Cl.⁷ **H01L 21/44**
(52) U.S. Cl. **438/614; 438/640**
(58) Field of Search **438/614, 622, 438/637, 640**

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Primary Examiner--Kevin M. Picardat
(74) Attorney, Agent, or Firm--TrackBritt

(57) **ABSTRACT**

The present invention relates to an improved method for forming a UBM pad and solder bump connection for a flip-chip which eliminates at least two mask steps required in standard UBM pad forming processes when repatterning the bond pad locations.

15 Claims, 6 Drawing Sheets

